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Howard R. Huff

SILICON WAFERS for the MESOSCOPIC ERA

Howard R. Huff
International SEMATECH, Inc.
Austin, Texas 78741

Abstract. The biggest challenge facing the future of Front-End Processes at and beyond the 100 nm technology node lies in the fabrication of the basic transistor structure. That process will entail development of a higher-k gate dielectric and the associated processing of the gate stack as well as a highly-doped, ultra-shallow junction contacting the advanced transistor structure. The smaller dimensions associated with continued transistor scaling, moreover, offer the opportunity for a detailed re-examination of the role and usefulness of silicon wafer specifications. Data is being developed that suggests a reduction of various contaminants and defects as well as the continued reduction of certain other wafer specifications in silicon wafers may not necessarily be required to ensure continued improvements in IC performance, although detailed yield and reliability studies are still required to fully quantify these observations. The innovative transistor structures being fabricated in three-dimensional device configurations (which may be regarded as the natural evolution of the multi-zone wafer design concept), may further de-couple the starting silicon wafer from the active transistor structure. The implications of these transistor requirements on the silicon wafer for the ensuing mesoscopic (i.e., ≈ a few 10's nm) era may offer significant cost-of-ownership (CoO) opportunities in the relevant wafer specifications.

INTRODUCTION

The pervasiveness of the microelectronics revolution has continued apace for the past 40 years with integrated circuit (IC) density quadrupling every three years (1-3) in conjunction with improved transistor performance (e.g. speed). Device scaling has been the engine driving this revolution (4-7) with transistor gate delay approaching ≤ 1 ps for gate length critical dimensions (CDs) ≤ 40 nm (8,9). The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) (10) is anticipating 35 nm design rules by 2014. Figure 1 compares the lithographic CD trends from 1994, 1997, 1998 and 1999, wherein each succeeding Roadmap has pulled in the Technology Generation by one year. MOS transistor switching has already been demonstrated to ≈ 18 nm, with possible scaling to 10 nm in an innovative transistor configuration (11). The decrease in operating voltage, V_{DD}, is of especial importance, reducing the propensity for gate dielectric leakage, p-n junction breakdown and latch-up (12,13).

Concurrently, the development of advanced transistor structures utilizing material configurations such as silicon-germanium strained layers for the channel in conjunction with SOI (14), selective epitaxial silicon channel structures on silicon (15) and innovative vertical transistor structures have been accelerating (16,17). The role of quantization in these ultra-submicron structures will also need to be assessed (18). The continued evolution towards 3-D device integration is regarded as a significant step (i.e., ≈ a few tens nm) era (19,20). These innovative transistor configurations, which may be regarded as the natural evolution of the multi-zone wafer design concept (21-26) will further de-couple the starting silicon wafer from the active transistor structure and may offer significant cost-of-ownership (CoO) opportunities in the relevant wafer specifications. In these cases, the device active regions are selectively tuned by the fabrication of zones appropriate to the device functions.

In that regard, CoO is traditionally associated with the capital equipment, which an IC company owns, operates and depreciates. The contribution to the final product cost (measured in \$/wafer or \$/cm^2) of using a certain tool is a metric which can be used to drive improvements in the equipment productivity and also understand the trade-offs between competing cost factors such as depreciation (i.e., price), consumables, operators, etc. so that a company can select the tool which meets its operational strategy. By analogy, the CoO for a silicon wafer (which is a direct material for an IC company) can be assessed in two ways. First, its contribution to the final product cost is measured, again, in \$/wafer or \$/cm^2, and the associated analysis of the contributing factors to that cost such as excessively restrictive wafer specifications, extra measurements or processing, rising cost of poly … and, additionally, the balancing of the product wafer cost with the silicon wafer. The second contribution, in fact, goes beyond the CoO-level of analysis and requires utilization of the cost resource model (CRM).

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This occurs because the CoO for a tool, for example, does not include the burden of that tool's demanding a more expensive wafer or that tool's obviating an expensive feature of a wafer, such as starting metals or flatness. The CRM analysis places a cost on the whole IC process, including tools and wafers, so it can be used to understand these higher-level trade-off issues (27).

Silicon (28) and silicon-based materials such as silicon-germanium have been and will continue to be the vehicle for continued IC scaling (26) and mainstream CMOS structures with applications far beyond the next 15 years. Although alternative material and device configurations may be utilized for sub-10 nm applications based on a "disruptive new technology" (29), silicon-based materials will continue to be utilized for those applications not necessarily requiring state-of-the-art design rule structures throughout the 21st century.

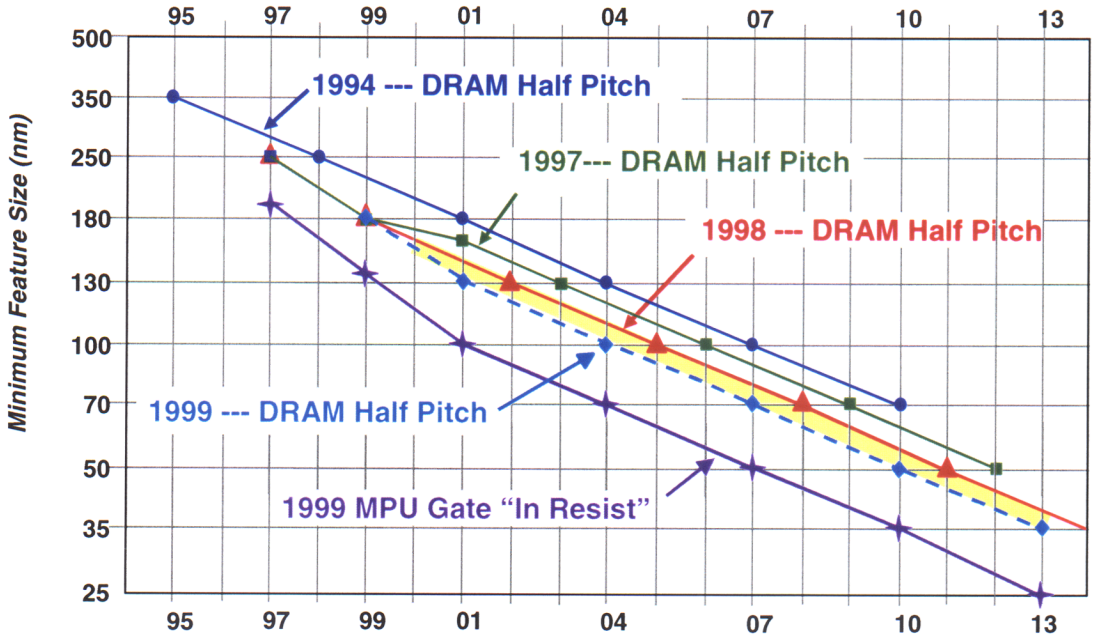

FIGURE 1. SIA roadmap acceleration analysis (from Lithography Technical Working Group Summary) (10).

MOS INTEGRATED CIRCUIT TRENDS

The switching speed of the metal-oxide-semiconductor (MOS) oxide- transistor has been decreasing for more than 30 years by reducing the size of the MOS transistor, with gate delays approaching ≤ 1 ps for gate lengths less than ≈ 40 nm (8,9). MOS scaling theory requires all relevant vertical and lateral dimensions to be simultaneously scaled (7-9). Figure 2 illustrates the transistor device components pertinent to our discussion. These include: (a) gate stack, (b) source/drain extension, (c) isolation, (d) channel, (e) wells, (f) DRAM capacitor stack/trench (the location of the DRAM capacitor stack/trench in the substrate is still a viable option), (g) starting material and (h) contacts (10). Of course, the transistor structure and device configuration will evolve during the next 15 years (30,31). A summary of several key IC, transistor and MOSFET characteristics is summarized in Table 1.

Gate Stack

Silicon dioxide has been the prototypical gate dielectric for IC applications for 40 years for three primary reasons: (1) it serves as a *patternable mask* for the localized diffusion of commonly utilized dopants in silicon, forming a blocking, amorphous layer; (2) it *passivates* the silicon surface, with a surface-state density ≈ 1-3 x 10^{10} $(eV\text{-}cm^2)^{-1}$; and (3) it is an *insulator*, with a large energy gap ≈ 9 eV, and affords a convenient material for the deposition of adherent, conducting films connecting the various device components in the IC.

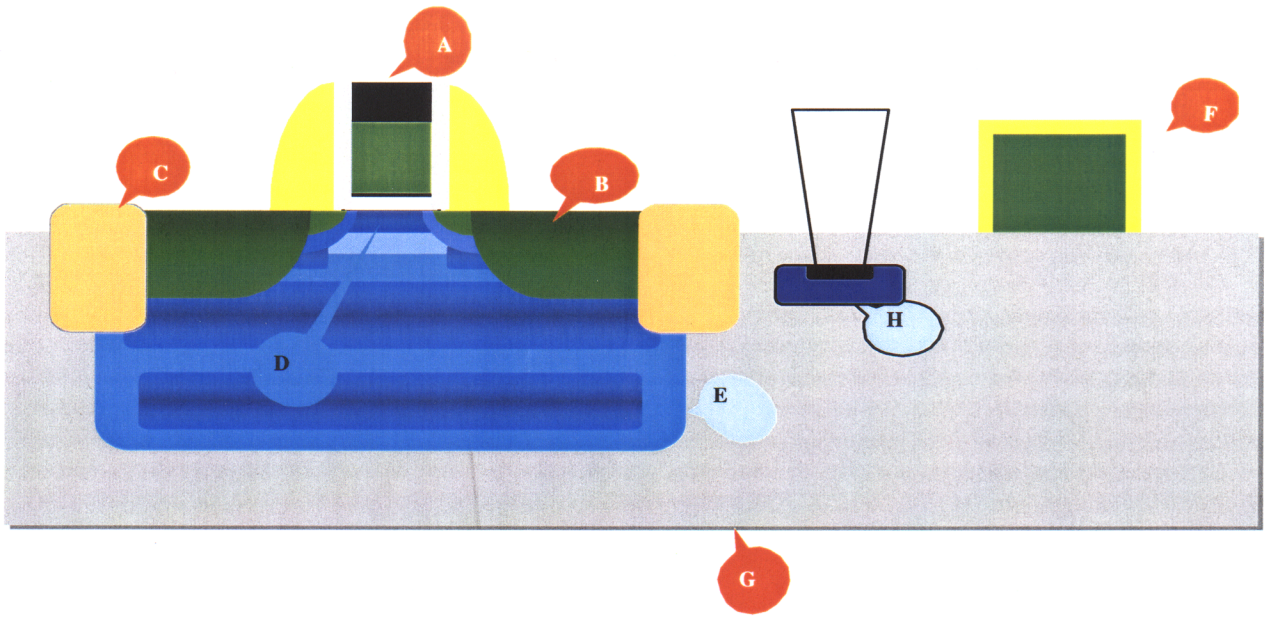

FIGURE 2. Transistor device components relevant for silicon wafer wafer specifications: (a) gate stack, (b) source/drain extension, (c) isolation, (d) channel, (e) wells, (f) DRAM capacitor stack/trench (the location of the DRAM capacitor stack/trench in the substrate is still a viable option), (g) starting material and (h) contacts (10).

YEAR	1999	2002	2005	2008	2011	2014
TECHNOLOGY NODE (nm)	180	130	100	70	50	35
DRAM 1/2 pitch (nm)	180	130	100	70	50	35
MPU Gate Length (nm)	140	85-90	65	45	30-32	20-22
CIRCUIT CHARACTERISTICS (HIGH-PERFORMANCE MICROPROCESSOR)						
Functions per chip (M transistors)	110	> 220 , < 441	882	2,494	7,053	19,949
Chip size at ramp (mm^2)	450	> 450 , < 567	622	713	817	937
Logic Transistors/cm^2 at ramp (M)	24	> 49 , < 78	142	350	863	2,130
Clock Frequency, across-chip (MHz)	1,200	1,600	2,000	2,500	3,000	3,600
Maximum chip power with heatsink (W)	90	130	160	170	174	183
DEVICE CHARACTERISTICS (HIGH-PERFORMANCE MICROPROCESSOR)						
Power Supply Voltage V_{DD} (V)	1.8 - 1.5	1.5 - 1.2	1.2 - 0.9	0.9 - 0.6	0.6 - 0.5	0.6 - 0.3
Maximum I_{OFF} @ 25C (minimum L device) (nA/μm)	5	10	20	40	80	160
Nominal I_{ON} @ 25C (μA/μm) (NMOS / PMOS)	750 / 350	750 / 350	750 / 350	750 / 350	750 / 350	750 / 350
MOSFET DIMENSIONS						
T_{EOT} (nm)	2.5 - 1.9	1.9 - 1.5	1.5 - 1.0	1.2 - 0.8	0.8 - 0.6	0.6 - 0.5
Source / drain contact, X_J (nm)	145 - 75	90 - 45	70 - 35	55 - 30	40 - 20	35 - 15
Source / drain extension, X_J (nm)	70 - 42	43 - 25	33 - 20	26 -16	19 - 11	13 - 8

TABLE 1. Summary of Several Key IC (High-Performance Microprocessor), Transistor & MOSFET Dimensional Characteristics (10)

Indeed, scaling of the SiO_2 gate dielectric from 75-100 nm for the 4K DRAM in 1974 to anticipated values of an oxide equivalent thickness (T_{EOT}) of 1.0 - 1.5 nm for the 100 nm technology generation (for a high-performance microprocessor (MPU), has proceeded in conjunction with the scaling of the other device components. With the continued scaling towards and beyond the 100 nm technology generation, however, both the conventionally fabricated gate dielectric and the shallow junction technologies are reaching significant technical barriers.

For example, as we approach the 100 nm technology generation ($T_{EOT} \approx$ 1.0-1.5 nm), the direct-tunneling gate leakage current, I_{gate}, for SiO_2 films is comparable to the NMOSFET off current, I_{off}, (32-34), thereby increasing the off-state power level of the circuit, see Figure 3 (32-34). In this regime, an approximately 0.1 nm decrease in SiO_2 thickness corresponds to $\approx$ one-half order of magnitude increase in gate leakage current density. Even though transistors can still function where I_{gate} and I_{off} are comparable, the power associated with the sum of those currents must stay below a limit for stand-by power consumption (an extremely important factor in increasingly complex mobile electronics). Circuit level failure may result, however, because the IC design generally assumes no appreciable gate current. On the other hand, the most cost-effective near-term solutions for the IC industry may include circuit design solutions such as ultrathin SiO_2 for only the critical nodes, critical re-assessment of the gate dielectric leakage current requirement (35), more power-tolerant IC designs as well as sophisticated power management schemes (36).

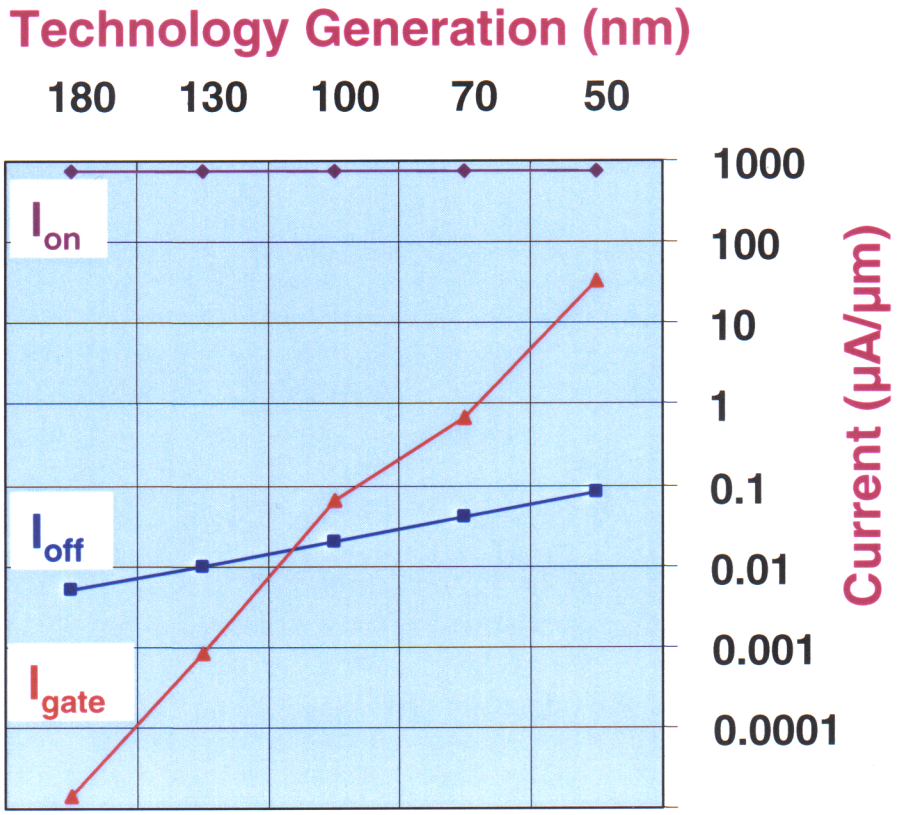

FIGURE 3. I_{on}, I_{off} and I_{gate} (μA/μm) versus technology generation (32-34).

Accordingly, the intrinsic performance of SiO_2 may be more limited by fundamental material properties in sub-2 nm gate oxides, where the number of SiO_2 layers is less than six (37), rather than contaminants such as metals and residual structural defects such as crystal originated pits, COPs (38). An additional component of leakage current which must be addressed is that arising from root-mean-square (rms) fluctuations in surface microroughness (see section on Microroughness).

An alternative gate dielectric with dielectric constant greater than that of SiO_2 (k= 3.92) has been proposed (39-43) to obviate the IC power concern, while still achieving the required gate electrode capacitive coupling with silicon.That is, T_{EOT}, [T_{EOT} = {$3.92/k$} x T_{PHYS}], may still be scaled which will also increase the transistor drive current, I_{DSAT}. The higher material, however, introduces a new set of design constraints (44). Finally, because of direct tunneling, I_{gate}, is not sensitive to temperature. Methodologies such as alloyed oxynitride layers (45) or higher-k dielectric layers as noted above (41-43) can be used to control this leakage current. Therefore, it turns out that I_{gate} can be significantly less than I_{off} at IC operating temperatures of $\approx$ 110°C (46).

The use, initially, of an oxynitride (followed, perhaps, by a silicon nitride gate dielectric) with a polysilicon gate electrode may constitute the initial step beyond the SiO_2-polysilicon gate electrode configuration, thereby possibly delaying implementation of the higher-k dielectric gate stack to beyond the 100 nm technology generation (47,48). While the IC manufacturing cost is recognized as a significant factor for sub-100 nm technology generations, the gate dielectric (and associated processing of the gate stack) is generally recognized as the major technological factor, although the complexity (and cost) of IC designs will surely escalate.

Channel Doping

Scaling is not only required for the gate dielectric to ensure continued improvement in I_{DSAT}, but is also required for the transistor's gate (channel) length to increase the transistor's switching speed (interconnection delays are not considered in this front-end perspective). Device scaling of the gate (channel) length has evolved from $\approx$ 7.5 μm for the 4K DRAM in 1974 to anticipated values of $\approx$ 65 nm for the 100 nm technology generation (for a high-performance MPU). Increased capacitive coupling of the gate electrode to the channel (by reduced T_{EOT}) can be accommodated with an increased dopant concentration in the channel (introduced by ion implantation, for example). This can ensure further scaling of the transistor's gate (channel) length, due to the increased channel barrier as a result of the improved isolation between the source and drain, while still retaining a low I_{off} (12,13). A major challenge for continued scaling, however, is that transistor dimensions will become so small that statistical fluctuations in the number and distribution (positioning) of dopant atoms in the channel (and free-charges on the transistor gate) can induce significant changes in device and IC behavior (12,13,49).

Source Drain Doping

The source and drain dimensions (e.g., junction depth) are also scaled in the drive to the sub-100 nm transistor as seen in Table 1. Device scaling of the junction depth has evolved from several μm for the 4K DRAM in 1974 to anticipated values of $\approx$ 25 nm for the junction depth extension for the 100 nm technology generation (for a high-performance MPU). The total amount of charge in the source, drain and channel regions, however, must not decrease in order to maintain low device resistance (12,13). Since these dimensions are becoming smaller, transistor scaling requires an increase in the local donor and acceptor concentrations, as appropriate, in order to maintain a constant total charge in these regions. Unfortunately, the dopant concentration in the source and drain regions have approached about 1% of the silicon crystal density, resulting in the maximum thermodynamic solubility at the relevant fabrication temperature.

The ITRS device trends, requiring increased dopant concentrations (reduced sheet resistance) in these smaller localized regions, will therefore require new methodologies such as spike anneals (i.e., anneals exhibiting little to no dwell time at the peak temperature) to activate dopants to the required level. Material effects that must be accommodated include the non-equilibrium dopant incorporation and metastable dopant stabilization (without dopant cluster formation and related complexes that generally degrade transistor performance). It is critical for future device scaling that the total amount of charge on the source, drain and channel regions does not decrease in order to maintain low-device resistance, with no resulting loss of total charge and potential degradation in device performance (12,13, 48)

Several additional strands also require consideration. The reduction of the source/drain junction capacitance is receiving greater attention (46,50). Although the junction depth is decreasing with the reduction in CD, the active p-n junction length in the IC is increasing due to the continued

increase in the total number of transistors per chip (see Table 1). Accordingly, the total chip sensitivity to metals continues to require cognizance, although both cleaner chemicals and factories should be taken into account for CoO opportunities.

SILICON MATERIALS – CURRENT STATUS

Silicon material criteria and ASTM procedures for ensuring the electrical, chemical, structural and mechanical characteristics to support very large scale integration (VLSI), along with an extensive set of tables and figures have been reviewed (51). More recently, tailoring of silicon material characteristics to the requisite IC requirements through silicon wafer product design (52), emphasis on physics related characteristics of silicon (53,54) and a detailed account of silicon properties in comparison to other group IV semiconductors (55) have been reviewed. The global 300 mm initiative, furthermore, with its emphasis on standardization methodologies, has been instrumental in facilitating the onset of the 300 mm era (56) (see section on Future Material Directions - Large Diameter Wafers)

The conventional trend in silicon wafer characteristics for ultra large scale integration (ULSI) applications has often consisted of increasingly tighter specifications so as to match the current sensitivity limits of metrology tools. A shift occurred during the 1990's, however, with an increased emphasis towards the scientific understanding of the physico-chemical properties and processes in silicon, the selective application of design of experiment (DOE) methodologies and model-based silicon wafer criteria for the ITRS. Model-based experiments and simulation procedures became *de rigeur* in the IC industry and technology advancement was as much based on scientific principles as on experience per se. Accordingly, it became necessary to balance the "best wafer possible" against the CoO opportunity of not driving silicon requirements to the detection limit but to some less stringent value consistent with achieving high IC yield (57,58). Indeed, model-based silicon wafer criteria for optimal IC performance became the *le motif* of the industry (10). The wafer characteristics described in the ITRS were generally derived from a model-based analysis based on CDs, bits or transistors per chip, chip size, wafer size, etc. Although empirical models were employed as appropriate, anecdotal opinions were generally minimized. Since the parameter values are only as reliable as the underlying models, however, understanding of the models and the IC performance-characteristic relationships were generally viewed as more critical than the specific numerical values.

We shall examine several recent MOS device characteristics discussed in the literature and interpret these results in terms of their CoO implications for silicon (and silicon-germanium) wafer characteristics for ICs which are approaching mesoscopic dimensions. We will not, however, project the anticipated material(s) beyond silicon and silicon-germanium which will be required to extend digital switching technology beyond 10 nm for leading-edge computer and telecommunication applications. The inability (and, perhaps, inadvisability) of such projections to anticipate their applications was noted by Bob Wallace of Bell Laboratories (60-62) shortly after the invention of the point-contact and junction transistors and appears to still be valid. Indeed, it has recently been noted that "... there is no *a priori* [italicized in original] way to determine what will tip a market. It's a fundamental instance of chaos in group dynamics. And that makes it fundamentally difficult to predict future societal behaviors in the adoption of technologies. ... we'll never be able to predict which technologies will become market successes" (62).

WAFER SPECIFICATION TRENDS

SURFACE TRENDS

Metals

The implications of ultra-thin gate dielectrics on the specification of metals and COPs is significant and, paradoxically, may be less stringent than for the case of thicker gate dielectrics (63). A quantitative model of gate oxide breakdown suggests that a singular behavior is reached in the oxide thickness regime approaching 2 nm or so when the effective defect size becomes comparable with the oxide thickness (64).

The generic specification for metals such as Fe, Ni and Cu (65) has typically been about $10^{10}/cm^2$ for 180 nm design rule ICs (oxide thickness $\approx$ 1.9 - 2.5 nm) and has been projected to reach < $10^{10}/cm^2$ for sub-130 nm design rules (T_{EOT} < 1.5-1.9 nm), based on the assumption of extrapolating experimental data for oxides greater than 5 nm (10). Recent experiments on 5–17 nm oxides, however, indicate the reduced influence of critical metals such as Ni at $10^{11}/cm^2$ and higher on the charge-to-breakdown, Q_{BD}, a critical gate oxide integrity (GOI) parameter, with reduced oxide thickness as shown in Figure 4 (66,67). It has also been shown that stress-induced-leakage-current (SILC) becomes less sensitive for an Fe contaminated 3.5 nm oxide, compared to a 7.0 nm oxide (68). Investigations are required, however, to assess the implications of these observations for time-dependent dielectric breakdown (TDDB).

Furthermore, wet chemical cleaning efficiencies greater than 95% for critical metals such as Fe (69) have been demonstrated. Accordingly, an incoming metal specification of $\approx 10^{11}/cm^2$ may operationally result in $< 10^{10}/cm^2$ on the silicon surface after cleaning. Although it may be disconcerting to specify the incoming wafer critical metals in the range of $\approx 10^{11}/cm^2$, the viability of driving initial critical metals $< 10^{10}/cm^2$ may be inappropriate from a CoO perspective, even though most silicon suppliers can currently meet a specification in the upper $10^9/cm^2$ for most metals. On the other hand, it should be noted that with the potential onset of gate dielectric materials with dielectric constants significantly larger than SiO_2, these materials may require different pre- and post-gate surface preparation cleans and the metallic issue may require re-assessment.

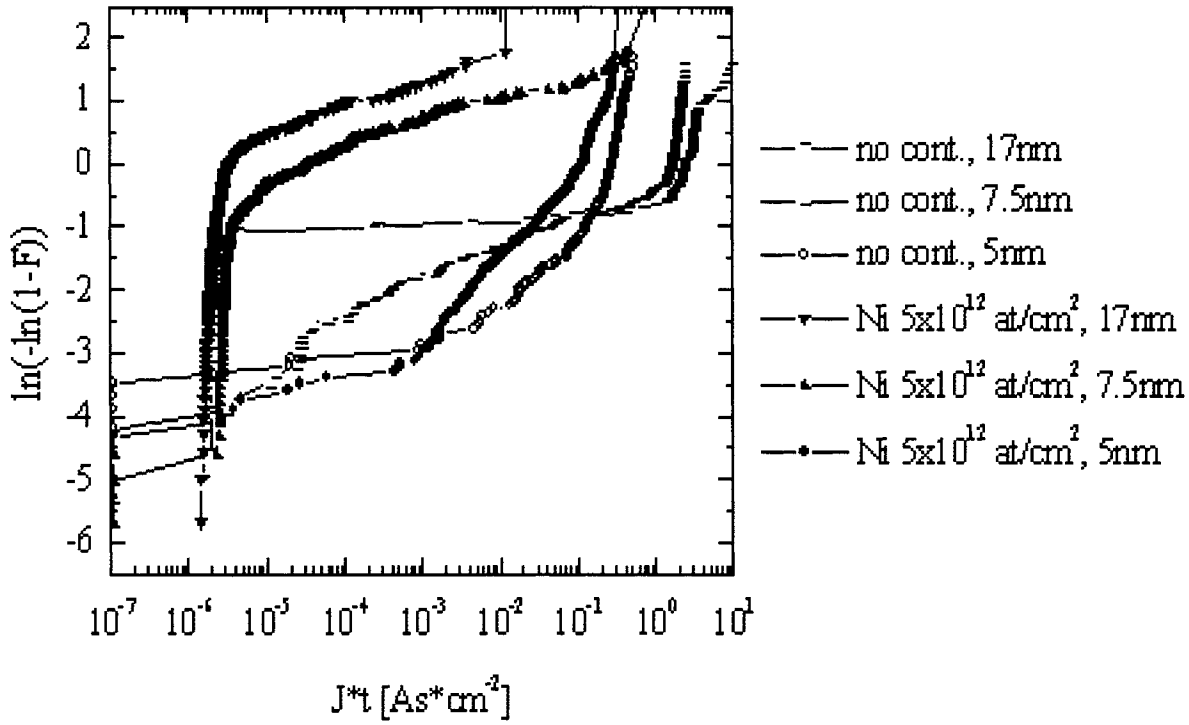

FIGURE 4. Dependence of the Weibull distribution with Q_{bd} for oxide thicknesses 5 nm, 7.5 nm and 17 nm for 10^{12} Ni/cm^2 (66). Reprinted, with permission, from STP 1382 – Gate Dielectric Integrity: Material, Process, and Tool Qualification, copyright American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428.

Particles

The physical structure of the wafer surface has emerged as a critical concern. Both polished and epitaxial wafers exhibit defects that must be controlled to achieve high IC yields. Critical polished wafer defects include surface chemical residues, such as organics, particles and COPs. Structural defects, such as epitaxial stacking faults and other large area defects, must also be controlled on epitaxial wafers (70). Material requirements are expressed in terms of specific types of surface defects. It is important to note that the total defect count is the sum of the various constituents. For example, both particles and COPs must be taken into account when considering the total surface defect density on Czochralski (CZ) polished wafers whereas epitaxial stacking faults and large area defects must be included for epitaxy wafers, in which case COPs are not relevant.

The removal and prevention of surface defects is a current state-of-the-art challenge for silicon wafer technology. The development of laser scanning and other instrumentation to count, size, and determine the composition and morphology of these defects is a critical metrology challenge, especially where the particle size is comparable to or less than the illuminating wavelength. In that regime, oscillations in the silicon particle scattering cross-section on a silicon surface versus the polystyrene latex (PSL)

sphere diameter (which is used to calibrate the laser surface scanner and also exhibits resonances) cause silicon sizing errors (71). The separation of particles and COPs continues to be of significant importance.

Similar considerations for particle density may be applicable as for metals when considering the wet chemical cleaning efficiency prior to thermal processing. It has also generally been considered, since the early '90's, that the critical particle size should be a fraction, originally 33% and currently 50%, of the design rule. Silicon suppliers have noted, however, that wafers supplied for the 180 nm technology generation apparently function quite well with the particle specification comparable to or as large as the design rule. On the other hand, one should not confuse what can be shipped (tolerable to the IC house) with what is needed to ensure optimal IC performance and yield. Nevertheless, taking the particle size equal to 90 nm (50% of the CD at the 180 nm technology generation) through the 130 nm node may not be as detrimental as previously envisioned due to an improved particle distribution (reduced mean and standard deviation). It is very useful from a metrology and CoO viewpoint, moreover, to specify the particle density required at a given CD in terms of the equivalent, smaller number of particles at a larger CD, as described by the (assumed) usual inverse square power law (72).

Finally, the chemical nature of the surface produced by the wafer supplier (hydrophobic versus hydrophilic) and the wafer-carrier interaction during shipment are important in controlling the subsequent adsorption of impurities and particles on the wafer surface. Especially important are organics, which are highly dependant on the wafer packaging and wafer storage conditions such as temperature, time and ambient and continues to receive extended attention (73,74). In view of the semiconductor fabrication facility participating in the deposition of organics (75), however, specification of the initial organics to less than one monolayer does not appear warranted.

Crystal Originated Particles(COPS)

The degrading influence of COPs on the capacitor defect density during time-zero breakdown for a 20 nm oxide is significant, as seen in Figure 5 (76). As the oxide thickness decreases to $\approx$ 5 nm, however, the influence of COPs and related flow pattern defects on GOI and capacitor defect density has been found to become negligible for CZ polished wafers (76-78) in comparison to thicker oxides. Indeed, GOI may be regarded as a useful diagnostic technique to determine the presence of COPS. Here also, TDDB studies are required, as there may be an effect of COPs in this case (79). Nevertheless, the efficacy of utilizing "perfect" CZ silicon (80), while a remarkable scientific achievement, must be re-assessed for future generations of ICs fabricated in polished wafers from a CoO perspective. Of course, there are additional issues besides GOI that must be considered, since COPs can also impact IC isolation and leakage failures (81-83). Epitaxial layers $\geq$ 100 nm or so, furthermore, essentially covers up COPs in lightly doped substrates, essentially negating their influence (76,84) while COP formation in heavily doped p-type substrate wafers is suppressed (85).

Microroughness

The "absolutely" minimum "SiO_2" thickness for an ideal Si/SiO_2 interface device structure has been suggested to be $\approx$ 0.7 nm, arising from the evanescent wave function penetration (i.e., quantum mechanical tunneling) of $\approx$ 0.35 nm from each surface of silicon into the dielectric (37). This corresponds to about three atomic layers of silicon in the oxide; in "reality," the two silicon atoms at the boundaries of the oxide are not completely oxidized, so the oxide is really one silicon layer thick. Adding $\approx$ 0.3 nm for the surface microroughness rms (R_{rms}) excursions due to a thermally grown oxide on epitaxial silicon and taking into account a "representative" thermal process budget of 1050°C for 10 s, which essentially adds a similar roughness at the "SiO_2"/silicon gate electrode interface (due to the conversion of the amorphous silicon gate electrode into polysilicon, similar in roughness as the lower interface), the practical SiO_2 thickness should be at least $\approx$ 1.3 nm (37). It has also been suggested "both roughening and smoothing can occur as independent mechanisms lead[ing] to the prediction of a limiting interfacial roughness which has now been experimentally verified to be about 0.3 nm" (86).

Indeed, research on the fabrication of 1.0 - 1.3 nm "SiO_2" with $R_{rms} \approx 0.15 \text{ nm} \pm 0.02$ nm has recently been achieved on epitaxial silicon (initial $R_{rms} \approx 0.07$ nm) via a modified $NH_4OH + H_2O_2$ wet clean (87). It is anticipated that the production of such films with 1.4 – 1.5 nm may be forthcoming, albeit nitrogen may be utilized in these dielectric films. The utilization of a UV-Cl_2 clean has further reduced R_{rms} to $\approx 0.1 \pm 0.01$ nm, with significant improvements in both Q_{BD} (88) and an increase in the (effective) tunneling barrier height (89). Oxide thicknesses in the range of 1.3 – 4.0 nm exhibited similar R_{rms} using the UV-Cl_2 clean (88). The influence of cumulative thermal processing during IC fabrication on R_{rms}, however, also requires cognizence since, as noted above, both roughening and smoothing can occur as independent mechanisms under some

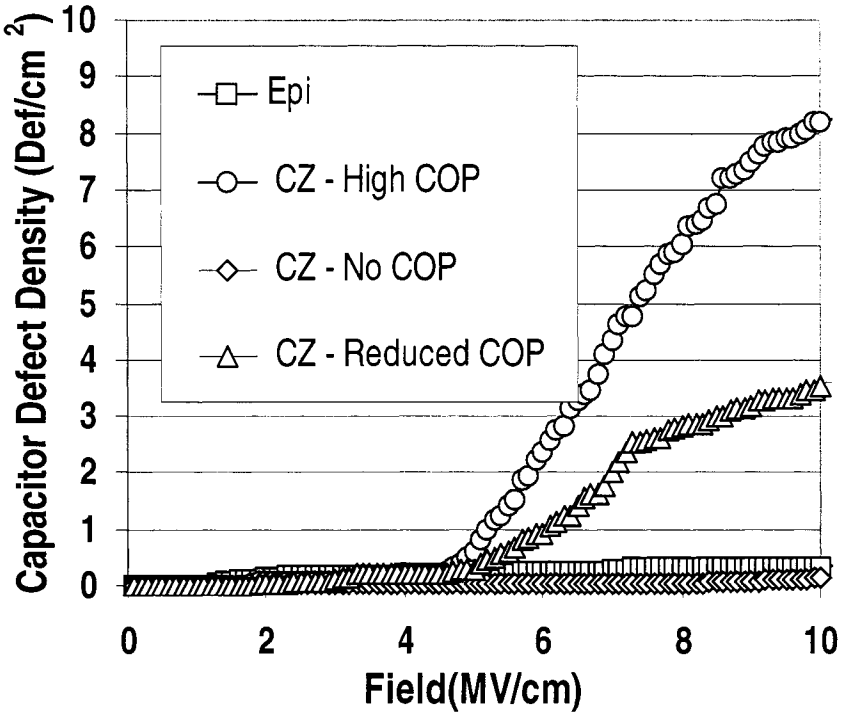

FIGURE 5. Capacitor defect density comparison for varying COP levels with 20 nm oxide (76). Reprinted, with permission, from STP 1382 - Gate Dielectric Integrity: Material, Process, and Tool Qualification, copyright American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428.

oxidation conditions (86). Accordingly, the viability of driving the initial $R_{rms} < 0.1$ nm, which can readily be achieved today, may not be justified from a CoO viewpoint.

Metrology issues are of significant importance for ultra-thin gate dielectrics. For example, scanning tunneling microscopy (STM) is a more meaningful measure of R_{rms} than atomic force microscopy (AFM) because the former is sensitive to the electronic distribution at the surface. The utilization of the range, rather than the standard deviation, is also more meaningful in characterizing ultra-thin gate dielectrics, inasmuch as the latter is a mathematical fit to the experimental data distribution (90). Finally, utilization of the power spectral density (PSD) may be a more useful representation of the surface microroughness, by integrating the PSD over the requisite surface wavelength (frequency) regime (72,91).

Flatness

The metric for site flatness should be matched to the type of exposure equipment used in leading edge applications. For the 180 nm technology node, full-field steppers with square fields (22 x 22 mm) are utilized and the site front-surface least squares total indictor range (SFQR) is the appropriate metric (92), which is taken equal to the CD. For the 100 nm technology node to the end of optical lithography, scanners will be utilized with maximum rectangular fields (25 mm x 32 mm) and the scanning front-surface least squares total indicator range (SFSR) may be the appropriate metric (92). Partial sites should be included in these specifications.

The SFSR metric typically results in a mean flatness value sufficient to accommodate the next smaller technology node (corresponding to SFQR) for the same field size, reflecting the greater topographic accommodation of scanners compared to steppers (93). Indeed, scanners are used at the most critical process levels with steppers used for the non-critical processes. The wafer flatness, however, continues to be a perturbation to lens aberrations and related lithography tool components (94) even as the industry continues its relentless pursuit of resolution enhancement technologies (95). The development of vertical transistor structures without the (eventual) limitations of optical lithography are also in progress. Accordingly, although ITRS flatness metrics approximate the CD for dense lines (DRAM half-

pitch), utilization of SFQR > CD may offer a significant CoO opportunity, consistent with an earlier SEMI epitaxial standard (96). The utilization of extreme ultraviolet lithography (EUVL) or x-ray lithography (XRL) wherein the wafer flatness is no longer critical due to the increased depth-of-focus (DOF) of ≈ 1 μm and ≈ 2 μm, respectively (97), continues to be discussed, although the utilization of these lithography tools, especially the latter, may only be for niche applications.

Nanotopography / Waviness

Flatness metrics define the calculation of the focal plane deviation of a field from a topography measurement via generic models of exposure tool focus/leveling mechanisms. Flatness metrology requires sufficient spatial resolution to capture the topological features relevant for each technology node and application (97). The vertical height of ≈ a few 100's of nm's in the case of optical lithography implies that spatial wavelengths (and resolution) of 1 - 2 mm are sufficient to capture the relevant vertical height excursions. However, to capture "nanotopology" features which may affect chemical mechanical polishing (CMP) at the 130 nm node, spatial wavelengths (and resolution) as small as ≈ 0.5 mm (with vertical heights ≈ $10 - 10^2$ nm) should be utilized in flatness topography measurements for the most comprehensive characterization.

WAFER SPECIFICATION TRENDS
SUBSTRATE TRENDS

Resistivity

The utilization of multiple-well structures fabricated by ion implantation in effect de-couples the transistor from the original silicon material characteristics, thereby reducing its sensitivity to the initial resistivity, tolerance and uniformity for both CZ polished and epitaxial substrate wafers (63). Whereas the nominal substrate doping for epitaxial wafers is typically in the range of ≈ 5-10 mΩ · cm to ensure latch-up control, shallow trench isolation (STI) is rendering classical concerns for latch-up, such as the n^+-p^+ spacing (admittedly becoming smaller), moot. The potential utilization of an implanted ground plane (high-dose barrier layer) in a polished wafer to prevent latch up and to getter impurities, rather than an epitaxial p/p^+ structure, has also received attention although its perceived benefits remain debatable in some cases and the control of COPs will be required in polished wafers. Accordingly, substrate resistivity ranges ≥ 20% may not be inappropriate, favorably impacting CoO.

The p^-/p^- epitaxial structure has also received attention for advanced IC applications, although this material configuration does not exhibit the solubility-enhanced iron gettering capability of heavily boron doped substrates (98). In the absence of solubility-enhanced gettering as in the mainstream epitaxial p^+ and p^{++} substrate wafers, the role of oxygen (as well as carbon and nitrogen) will have to be reassessed (99) since IG exhibits a higher density of bulk microdefects (BMDs) in actual processes for p^+ and p^{++} substrates as compared to p^- substrates (100-101). The p^-/p^- approach may, therefore, require re-tuning of the oxygen precipitation kinetics in the case of the p^- substrate. The perceived CoO opportunities may be beneficial, however, compared to 300 mm polished and especially p/p^+ epitaxial wafers as well as, perhaps, the benefit of reduced system capacitance as compared to utilizing heavily-doped substrates.

Finally, it should be noted that for an epitaxial layer resistivity greater than a few ohm-cm, a back-surface seal has generally been considered to be required for p/p^+ and especially for p/p^{++} structures. This approach minimized the transfer of the heavily-doped boron species, for example, from the wafer back surface and its deleterious transport to other regions of the IC and the tool equipment, especially when a film of polysilicon was utilized on the back surface for external gettering (EG) purposes (102). The utilization of both lower IC thermal process temperatures and double-side polished wafers, however, may negate the requirement of a back-surface seal.

Wafer Back-Surface

The back surface of the wafer is increasingly being polished to reduce particle contamination, improve wafer flatness, and increase wafer strength. This requirement may therefore enhance the importance of internal gettering (IG), as compared to EG (see section 3.2.3). The polished back surface, furthermore, may more readily exhibit microscopic contamination and handling scratches; ironically, a cleaner surface may actually appear to be dirtier. More stringent robotic handler standards may be required to ensure conformance with the implicit back-surface cleanliness requirements. Flatness degradation due to the presence of back-surface particles, which were previously hidden within the back-surface roughness, may also require consideration. Many EG techniques may also degrade the quality of the polished back surface and, in the case of non-uniformities in deposited-film-based EG,

may degrade the wafer flatness. Such EG techniques may be inappropriate. An initial approach for modeling the requisite back-surface particle size has been incorporated in the Starting Materials section of the ITRS (10).

Oxygen and Bulk Microdefect Centers

Internal gettering (IG), also referred to as relaxation gettering (98) in CZ polished silicon wafers, may still be required to remove deleterious metallic contaminants inadvertently introduced during IC processing. The formation of spatially uncontrolled SiO_x precipitates in the silicon substrate, possibly intersecting trench DRAM capacitors, for example, is likely to result in excessive device leakage current, necessitating attention to the magnitude and uniformity requirements for oxygen in silicon substrates to ensure stringent bulk defect control and homogeneous IG capabilities. Since the appropriate oxygen concentration significantly depends on the IC thermal process sequence to be employed, however, many factors must be considered in the selection of the optimal oxygen concentration, especially in the case where STI is greater than the epitaxial layer thickness. A $\pm$ 2 ppma variation in bulk oxygen concentration in the range $\approx$ 18-31 ppma (old ASTM standard) may be sufficient to ensure bulk defect control with acceptable IG capability. Adequate wafer strength and resistance to warpage, along with denuded-zone (DZ) width control, is also required.

Methodologies have recently been developed, moreover, wherein IG is independent of the bulk oxygen concentration, the details of the crystal growth process and, to a large extent, the details of the IC Fab thermal processes, but essentially dependent on the local vacancy concentration in the thermally treated wafer prepared by the silicon supplier (103). The ITRS suggests that BMDs for IG in polished wafers should be $> 10^8/cm^3$ (or $< 10^7/cm^3$ in the case of no IG) after IC processing. These number densities, however, were based on a limited set of experiments; more importantly, they are sensitively dependent on the cooling rate of the silicon wafers as well as the choice of polished or epitaxial wafer, where solubility gettering driven by the Fermi energy in the latter case becomes significant (98). That is, the utilization of a heavily doped p-type substrate for epitaxial applications offers an effective CoO gettering system via the Fermi effect (104).

Models are now being developed incorporating the thermodynamic (solubility) and kinetic (transport) factors whereby the IG BMD density may be specified depending on the details of the IC thermal processes, the metal species being gettered, the width of the DZ and the Fermi energy in the substrate (105). For example, speeding up the wafer cool-down process may preclude reaching thermodynamic solubility at lower temperatures, even in the presence of a IG BMD density sufficient for slower cool-down procedures. Figure 6 illustrates a model calculation for an epitaxial p/p^+ wafer with a fast cooling rate of 30°C/min, indicating an IG BMD getter center density as high as $\approx 10^{11}/cm^3$ is required to ensure that thermodynamic solubility of Fe is achieved at $\approx$ 700°C; the associated kinetics are also illustrated (106). The classical time-temperature-transformation (TTT) rate for epitaxial wafers with and without EG has been modeled (106) as well as the interactive effects of the substrate Fermi energy and IG (104,106).

EPITAXY

The improved gate dielectric integrity in epitaxial material is due to the lack of residual polishing micro-damage and COPs, both of which occur in polished wafers. However, the presence of extended area defects and epitaxial stacking faults can also degrade the gate dielectric integrity so these defects must also be carefully controlled (70). On the other hand, oxidation induced stacking faults are a minor occurrence in epitaxial films and may generally be ignored.

The reduction of the epitaxial-to-polished wafer cost ratio for 300 mm diameter wafers favors the continued use of epitaxial wafers for logic applications and may signify its use for other applications, such as memory circuits that have typically been manufactured on lower-cost CZ polished wafers. In that regard, the utilization of "perfect" CZ polished wafers (81) as a replacement for epitaxial wafers may be a viable alternative although CoO considerations and other wafer alternatives such as the H_2 annealed wafer will require consideration (see also section on Substrate Trends-Resistivity).

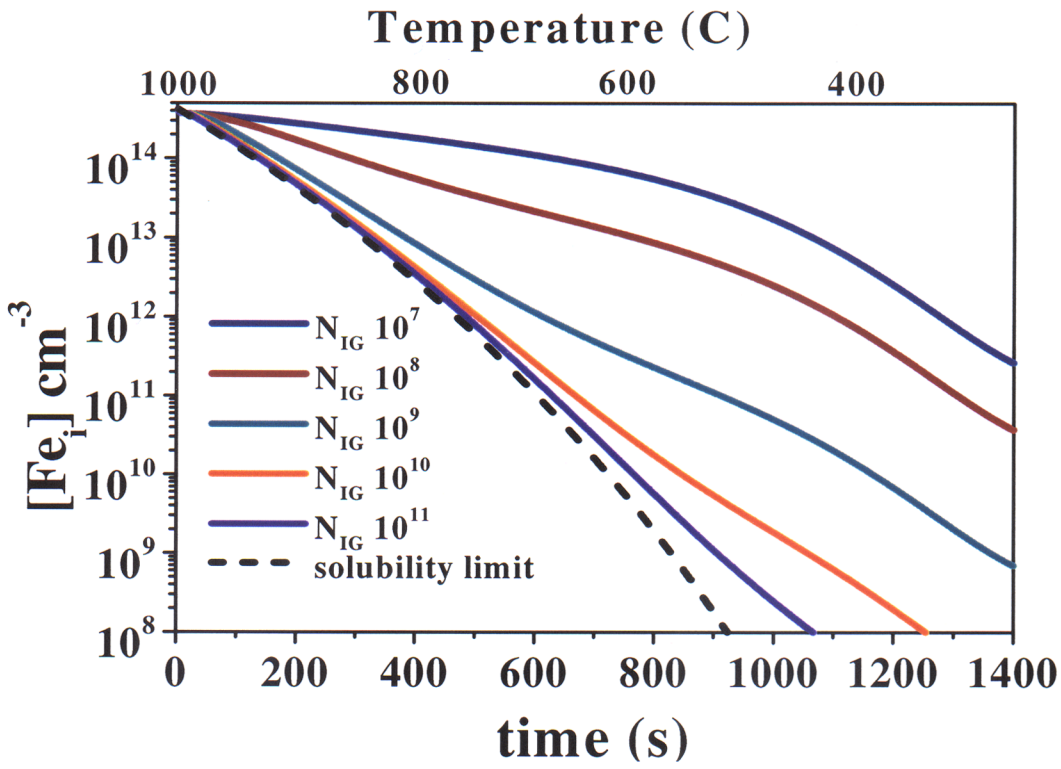

FIGURE 6. Gettering effectiveness of interstitial Fe with temperature and time with IG BMD site density, N_{IG}/cm^3, as a parameter for an epitaxial p/p^+ wafer. An increase in N_{IG} increases the equilibration rate (106). Reproduced by permission of The Electrochemical Society, Inc.

FUTURE MATERIAL DIRECTIONS

Large Diameter Wafers

The conversion to 300 mm diameter wafers, which began slowly in 1999 (peak conversion is anticipated ≈ 2001–2002) is necessary to achieve the required economy of scale for large volume IC manufacturing. International cooperation and standardization of wafers, carriers, and factory protocol continue to be critical for achieving this conversion in a cost-effective and timely manner. Business issues are the primary migration concern as it appears the engineering issues associated with cost-effective 300 mm crystal growth and wafer gravitational stresses can be addressed. For example, a reduced growth rate for 300 mm crystals is required, compared to 200 mm crystals, to ensure the removal of the increased total heat of solidification at the solid/liquid interface of the larger diameter ingot, while still ensuring single-crystal growth (107).

Projections of the next wafer diameter, based on an approximate doubling of the wafer area (10), suggests that 450 mm may be the next appropriate size at 2014 (some consideration in 2011 is under discussion), although development costs and related economic issues may be overwhelming (108,109). Indeed, technology barriers show up after rising costs have gone beyond the bounds of economic sense (110). The acceleration of technology generations and related economic factors, however, may cause the introduction of 450 mm diameter wafers to occur later than is currently projected. Continuation of the present wafer-diameter trend would also require the implementation of research in 2011 to drive the introduction of 675 mm diameter wafers in ≈ 2020. The 450 mm and 675 mm diameter wafers are projected to be approximately 1 mm thick, but significant gravitational stress and related equipment platform issues are anticipated with these larger diameter wafers. It is far from clear, however, whether either the 450 mm or 675 mm diameter wafers will be economically viable. A more effective growth opportunity for the IC industry may be the continued implementation of methodologies to enhance the overall equipment effectiveness (OEE) (111). In any case, a paradigm shift in the preparation of cost-effective silicon substrates will be required to mitigate the escalating costs associated with conventional silicon substrate materials. One possible

approach is the fabrication of silicon materials on an appropriate substrate so that it is not necessary to remove more than half the bulk silicon wafer to conform to IC package dimensions.

Silicon-on-Insulator (SOI)

Silicon-on-insulator (SOI) obviates the concern about latch-up while offering the potential for high-speed, low-power applications, soft-error immunity and, depending on the exact IC design details, possibly fewer process steps and smaller chip size. Different SOI approaches may be necessary to service different IC applications. Evaluation of the various SOI wafer fabrication techniques by material characterization and identification of the relationships between defects and SOI properties, defect control by gettering and the impact of defects on subsequent device properties, such as transconductance, buried-oxide breakdown voltage and leakage current, are essential. Although some bulk IC designs can be transferred directly to SOI substrates, process and mask redesign may further improve performance and reduce the chip size inasmuch as unique device configurations may be required. That is, different IC designs and applications require different layer thicknesses. Continued device scaling is expected to require new device structures such as fully depleted or double gate SOI devices. These devices will require thinner SOI layers and will, therefore, be more sensitive to layer thickness variations. The ability to create very uniform (< a few percent variation) thinner layers will be a catalyst for the use of such device structures. In any case, even if SOI does not extend the device scaling trends of the IC industry compared to conventional silicon materials (112), its benefits may motivate use for certain applications at a given technology generation. SOI is anticipated to enter the IC mainstream as a material system along with polished and epitaxial wafers, albeit dependent on the application.

SUMMARY

MOS transistor scaling continues to be the critical factor in improving IC density and performance, although more sophisticated scaling methodologies may be required (8). The smaller dimensions associated with transistor scaling offers the opportunity for a detailed re-examination of the role and usefulness of silicon wafer specifications. Recent literature data suggests that a reduction of various contaminants and defects as well as the continued reduction of certain other wafer specifications may not necessarily be required to ensure continued improvements in IC performance, although detailed yield and reliability studies are still required to fully quantify these observations. It would, of course, be advantageous to put this approach on a firmer basis. Unfortunately, in spite of about 40 years of IC fabrication, current models do not sufficiently establish the real requirements for parameter uniformity or the effects of parameter variability on IC properties (26, 113,114). Detailed understanding of silicon issues in relation to IC design and process technologies remains a significant scientific opportunity with far-reaching CoO implications. Development of such models, in conjunction with statistical specifications, is essential to enhance the utility of future Roadmaps.

DEDICATION

This article is dedicated to the memory of Dr. P.K. Vasudev.

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